

LINEAR INTEGRATED CIRCUIT

PRELIMINARY DATA

PREAMPLIFIER FOR CASSETTE RECORDERS WITH ALC

- EXCELLENT VERSATILITY in USE (V_s from 4 to 20V)
- HIGH OPEN LOOP GAIN
- LOW DISTORTION
- LOW NOISE
- LARGE AUTOMATIC LEVEL CONTROL RANGE
- GOOD SUPPLY RIPPLE REJECTION

The TDA 1054 is a monolithic integrated circuit in a 16-lead dual in-line plastic package.

The functions incorporated are:

- low noise preamplifier
- automatic level control system (ALC)
- high gain equalization amplifier
- supply voltage rejection facility (SVRF)

It is intended as preamplifier in tape and cassette recorders and players, dictaphones, compressor and expander in telephonic equipments, Hi-Fi preamplifiers and in wire diffusion receivers etc.

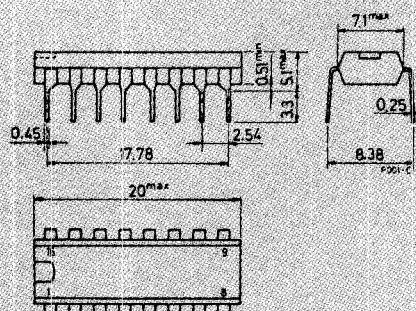
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
P_{tot}	Total power dissipation at $T_{amb} \leqslant 50^\circ\text{C}$	500	mW
T_{stg}, T_j	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

ORDERING NUMBER: TDA 1054

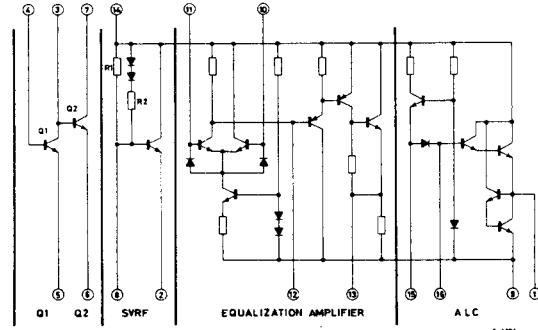
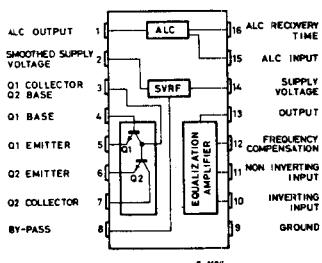
MECHANICAL DATA

Dimensions in mm

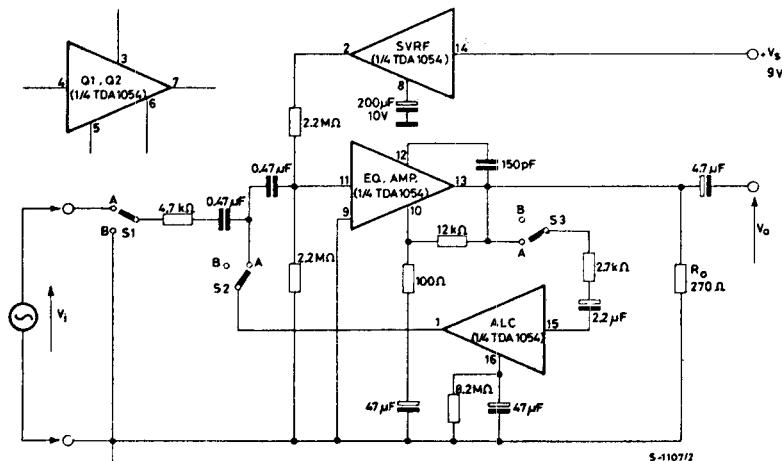


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CONNECTION AND SCHEMATIC DIAGRAMS



TEST CIRCUIT



THERMAL DATA

$R_{th\ J-amb}$	Thermal resistance junction-ambient	max 200	$^{\circ}\text{C/W}$
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ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_{amb} = 25^{\circ}\text{C}$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s Supply voltage		4	20		V
I_d Quiescent drain current	$V_s = 9\text{V}$ $R_o = \infty$ $S1 = S2 = S3 = B$		6		mA
h_{FE} DC current gain (Q1 and Q2)	$I_C = 0.1\text{ mA}$ $V_{CE} = 5\text{V}$	300	500		—
e_N Input noise voltage (Q1)	$I_C = 0.1\text{ mA}$ $V_{CE} = 5\text{V}$	2			$\frac{n\text{V}}{\sqrt{\text{Hz}}}$
i_N Input noise current (Q1)	$f = 1\text{ kHz}$		0.5		$\frac{\text{pA}}{\sqrt{\text{Hz}}}$
NF Noise figure (Q1)	$I_C = 0.1\text{ mA}$ $V_{CE} = 5\text{V}$ $R_g = 4.7\text{ k}\Omega$ $B(-3\text{ dB}) = 20\text{ to }10,000\text{ Hz}$		0.5	4	dB
G_v Open loop voltage gain (equalization amplifier)	$V_s = 9\text{V}$ $f = 1\text{ kHz}$		60		dB
V_o Output voltage with ALC	$V_s = 9\text{V}$ $V_i = 100\text{mV}$ $f = 1\text{ kHz}$ $S1=S2=S3=A$		0.95		V
R1 (for SVRF system)			7.5		$\text{k}\Omega$
R2 (for SVRF system)			120		Ω
e_N Equivalent input noise voltage (for equalization amplifier pin 11)	$V_s = 9\text{V}$ $R_g = 4.7\text{ k}\Omega$ $G_{v(closed)} = 100$ $S1 = B$ $B(-3\text{ dB}) = 20\text{ to }20,000\text{ Hz}$		1.3		μV
Drop-out (between pins 14 and 2)	$I_d = 6\text{ mA}$ $V_s = 9\text{V}$		0.8		V

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Fig. 1 – Equivalent input spot voltage and noise current vs. bias current (input transistor Q1)

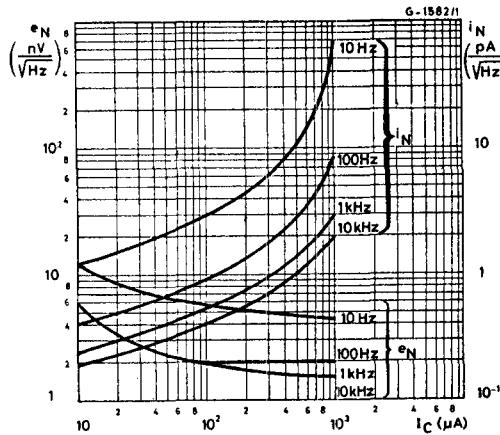


Fig. 2 – Equivalent input noise current vs. frequency (input transistor Q1)

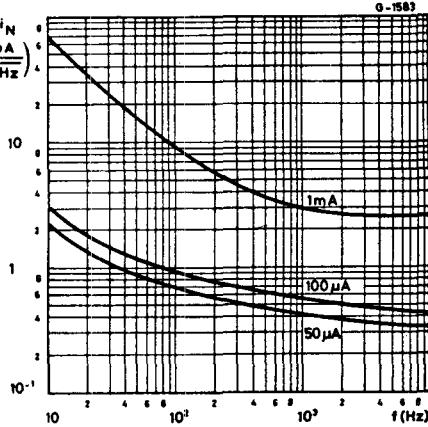


Fig. 3 – Equivalent input noise voltage vs. frequency (input transistor Q1)

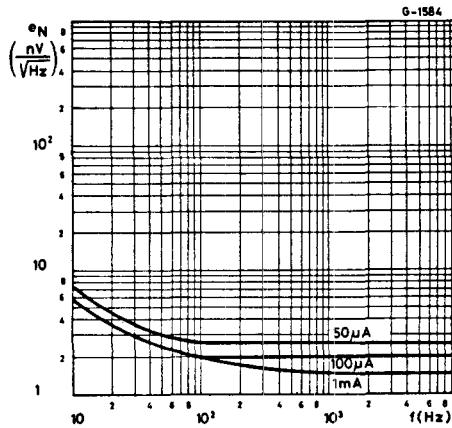


Fig. 4 – Typical noise figure vs. bias current (input transistor Q1)

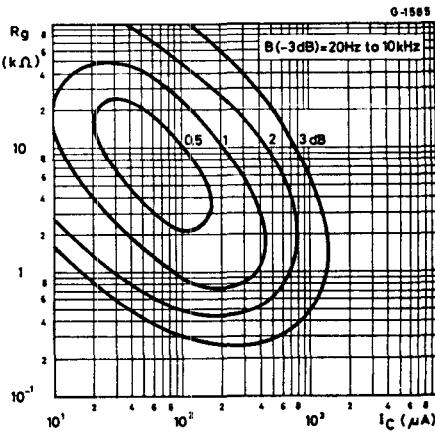


Fig. 5 - Optimum source resistance and minimum NF vs. bias current (input transistor Q1)

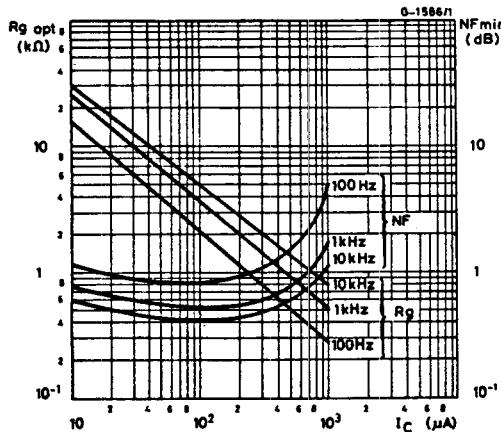


Fig. 6 - Typical current gain vs. collector current (input transistor Q1)

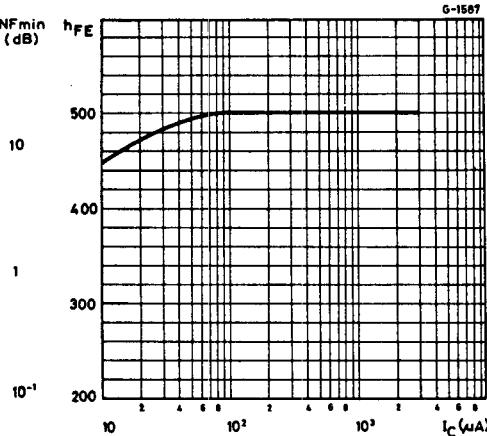


Fig. 7 - Typical open loop gain vs. frequency (equalization amplifier)

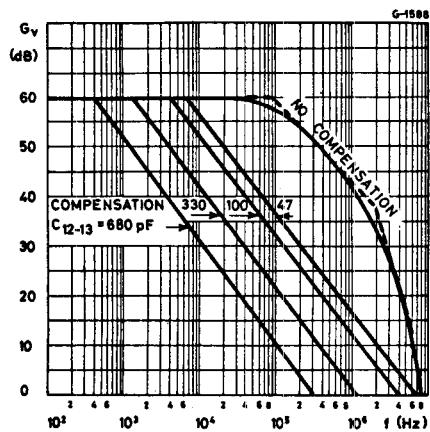
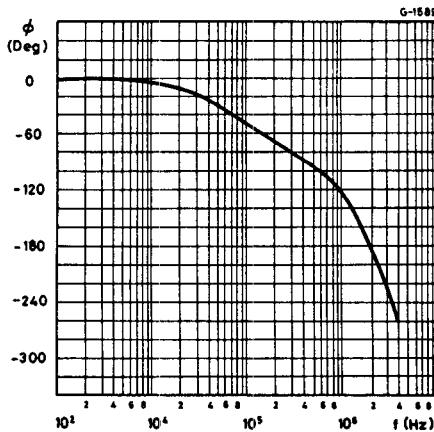


Fig. 8 - Typical open loop phase response vs. frequency (equalization amplifier)



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APPLICATION INFORMATION

Fig. 9 – Typical application circuit for battery–main tape and cassette player and recorder

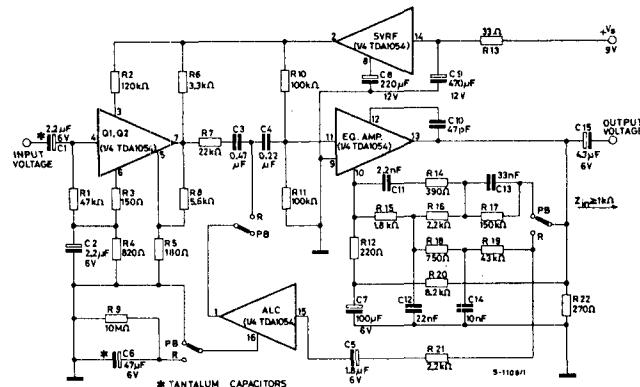
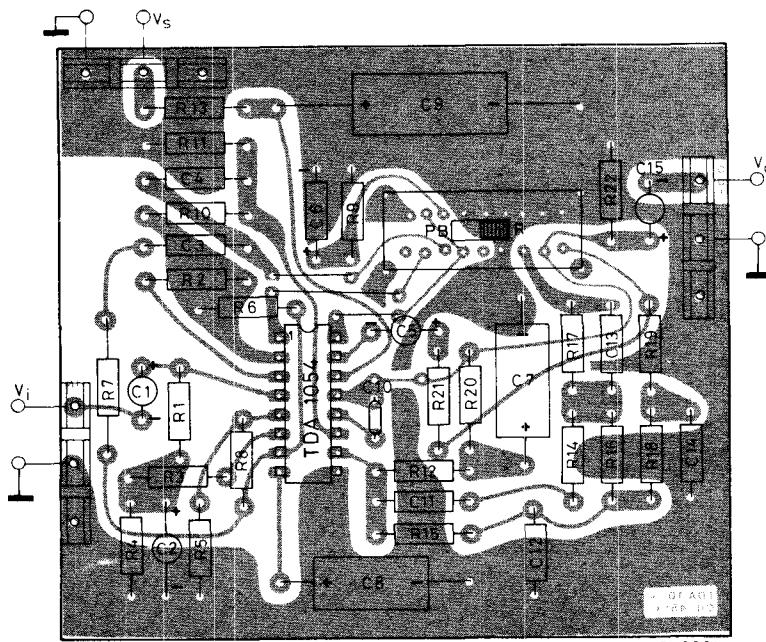


Fig. 10 – P.C. board and component layout of fig. 9 circuit (1:1 scale)



Typical performance of circuit in fig. 9 ($T_{amb} = 25^\circ C$, $V_s = 9V$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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PLAY-BACK

G_v	Voltage gain (open loop)	$f = 20$ to $20,000$ Hz	110		dB
G_v	Voltage gain (closed loop)	$f = 1$ kHz	57		dB
$ Z_i $	Input impedance	$f = 100$ Hz $f = 1$ kHz $f = 10$ kHz	10 41 43		$k\Omega$ $k\Omega$ $k\Omega$
$ Z_o $	Output impedance	$f = 1$ kHz	12	35	Ω
B	Frequency response			see fig. 12	
d	Distortion	$V_o = 1V$ $f = 1$ kHz	0.1		%
Output back-ground noise	$Z_g = 300 \Omega + 120$ mH (DIN 45405)		1.3		mV
			1.3		mV
$S+N/N$	Signal to noise ratio	$V_o = 1V$ $Z_g = 300 \Omega + 120$ mH	52		dB
SVR	Supply voltage ripple rejection at the output	$f_{(ripple)} = 100$ Hz	30		dB
t_{on}^{**}	Switch-on time	$V_o = 1V$	500		ms

RECORDING

G_v	Voltage gain (open loop)	$f = 20$ to $20,000$ Hz	110		dB
G_v	Voltage gain (closed loop)	$f = 1$ kHz	70		dB
B	Frequency response		see fig. 14		
d^*	Distortion without ALC	$V_o = 1V$ $f = 1$ kHz	0.3		%
d	Distortion with ALC	$V_o = 0.9V$ $f = 1$ kHz	0.4		%

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Typical performance of circuit in fig. 9 (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
ALC Automatic level control range (for 3 dB of output voltage variation)	$V_i \leq 40 \text{ mV}$ $f = 10 \text{ kHz}$	54			dB
V_o Output voltage before clipping without ALC	$f = 1 \text{ kHz}$	2.3			V
V_o Output voltage with ALC	$V_i = 30 \text{ mV}$ $f = 1 \text{ kHz}$	0.9			V
t_l^{**} Limiting time (see fig. 11)		75			ms
t_{set}^{**} Level setting time (see fig. 11)	$\Delta V_i = +40 \text{ dB}$ $f = 1 \text{ kHz}$	300			ms
t_{rec}^{**} Recovery time (see fig. 11)	$\Delta V_i = -40 \text{ dB}$ $f = 1 \text{ kHz}$	180			s
t_{on}^{**} Switch-on time	$V_o = 1\text{V}$	500			ms
$S+N/N$ Signal to noise ratio with ALC	$V_o = 1\text{V}$ $R_g = 470\Omega$	56			dB

* Measured with selective voltmeter

** This value depends on external network

*** When the DIN 45511 norm for the frequency response is not mandatory the equalization peak at 10 kHz can be avoided-so halving the output noise

Fig. 11 - Limiting, level setting, recovery time

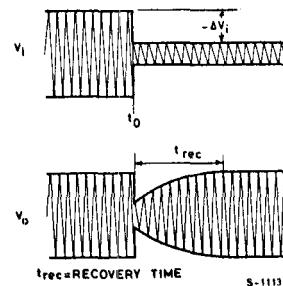
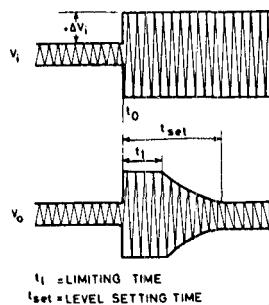


Fig. 12 - Typical relative frequency response of fig. 9 circuit (Play-back)

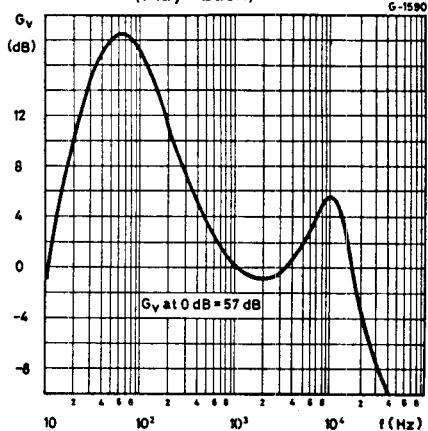


Fig. 14 - Typical relative frequency response of fig. 9 circuit (Recording)

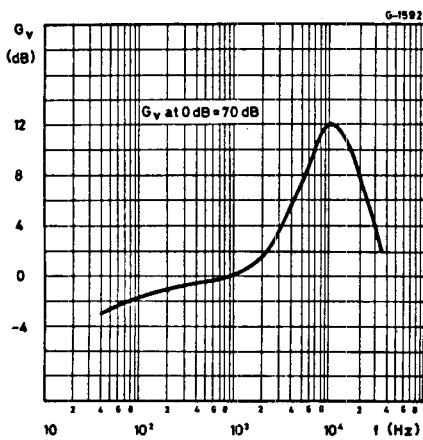


Fig. 13 - Typical distortion vs. frequency of fig. 9 circuit (Play-back)

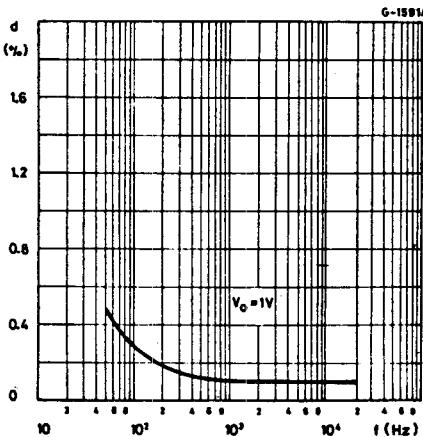
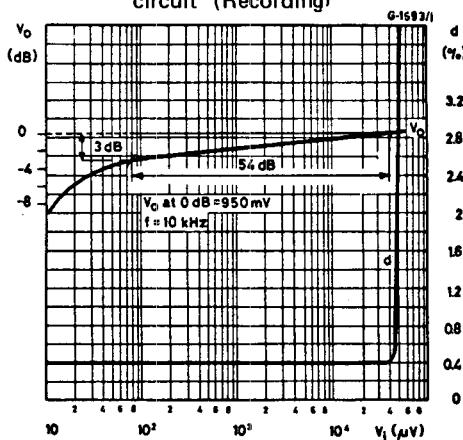


Fig. 15 - Typical output voltage variation and distortion with ALC vs. input voltage of fig. 9 circuit (Recording)



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Fig. 16 - Typical distortion vs. frequency with ALC of fig. 9 circuit (Recording)

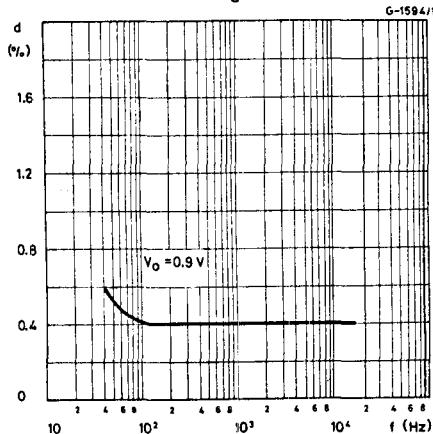


Fig. 17 - Typical limiting and level setting time vs. input signal variation

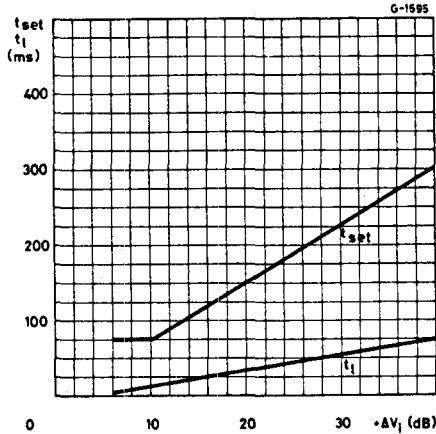


Fig. 18 - Economical application circuit

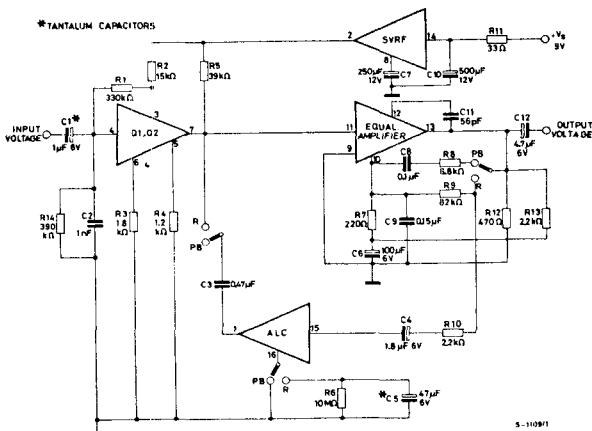
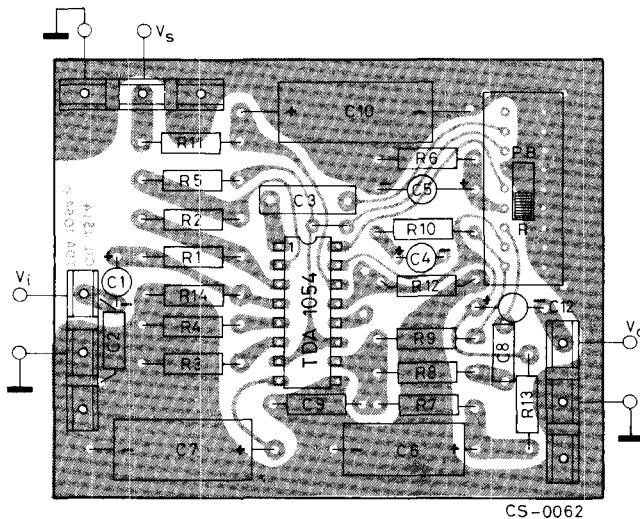


Fig. 19 – P.C. board and component layout of fig. 18 circuit (1:1 scale)



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Typical performance of circuit in fig. 18 ($T_{amb} = 25^\circ\text{C}$, $V_s = 9\text{V}$)

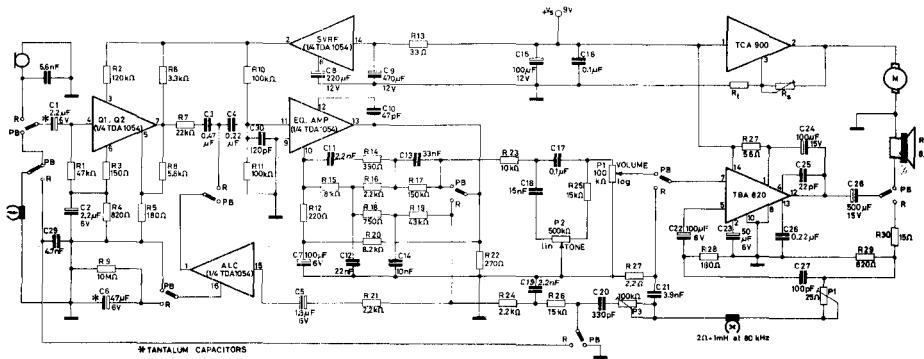
Parameter	Test conditions	Min.	Typ.	Max.	Unit
PLAY-BACK					
I_d	Quiescent drain current		18		mA
G_v	Voltage gain (closed loop)	$f = 1\text{ kHz}$	56		dB
B	Frequency response	$f = 100\text{ Hz}$ $f = 1\text{ kHz}$ $f = 6\text{ kHz}$ $f = 10\text{ kHz}$ $f = 60\text{ kHz}$	12 0 5 11 10		dB
d	Distortion	$V_o = 1\text{V}$ $f = 1\text{ kHz}$	0.6		%
Output weighted background noise		$Z_g = 300\ \Omega + 120\text{ mH}$ (DIN 45405)	1.3		mV

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Typical performance of circuit in fig. 18 (continued)

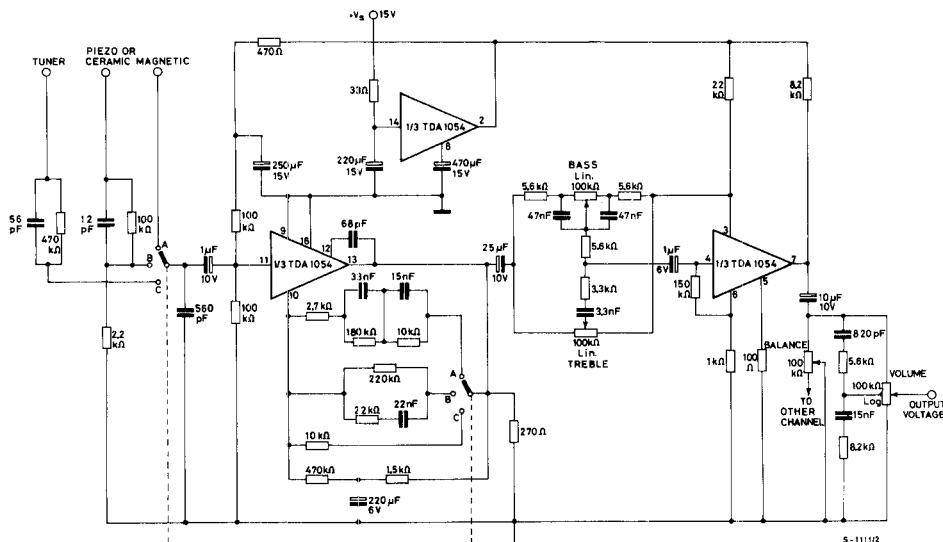
Parameter	Test conditions	Min.	Typ.	Max.	Unit
RECORDING					
G _v	Voltage gain (closed loop)	f = 1 kHz		70	dB
B	Frequency response	f = 140 Hz f = 1 kHz f = 10 kHz		-3 0 4	dB dB dB
d	Distortion	V _o = 0.9V f = 10 kHz		0.7	%
ALC	Range for 3 dB of output voltage variation	f = 10 kHz V _i ≤ 40 mV		54	dB

Fig. 20 - Complete cassette player and recorder



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Fig. 21 - Hi-Fi preamplifier for magnetic and ceramic pick-ups



Typical performance of circuit in fig. 21 ($T_{amb} = 25^\circ C$, $V_s = 15V$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s Supply voltage		10	18		V
V_i Input sensitivity for magnetic pick-ups	$V_o = 300 \text{ mV}$ $f = 1 \text{ kHz}$		2.5		mV
V_i Input sensitivity for ceramic pick-ups			100		mV
V_o Output voltage before clipping	$f = 1 \text{ kHz}$		2.5		V
RIAA equalization for magnetic pick-ups	$B = 40 \text{ to } 18,000 \text{ Hz}$		± 1		dB

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Typical performance of circuit in fig. 21 (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
$\frac{S+N}{N}$	$R_g = 4.7 \text{ k}\Omega$ $B (-3 \text{ dB}) = 20 \text{ to } 20,000 \text{ Hz}$		66		dB
$ Z_i $	$f = 1 \text{ kHz}$	47			$\text{k}\Omega$
$ Z_i $		470			$\text{k}\Omega$
$ Z_i $		100			$\text{k}\Omega$

Fig.22 - Typical distortion vs. frequency (fig. 21 circuit)

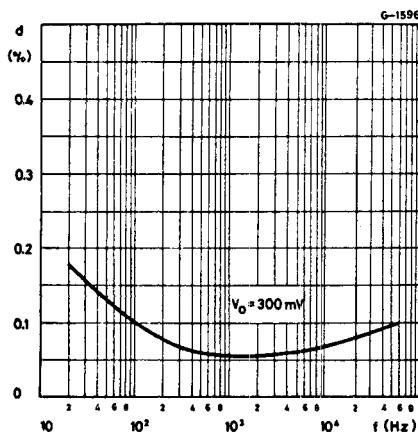


Fig. 23 - Typical frequency response (fig. 21 circuit)

